Listing of Claims:

1. (Original) A method for manufacturing a semiconductor device comprising:

forming gate lines on a semiconductor substrate;

forming a first insulating layer to cover the gate lines;

forming first contact pads and second contact pads, wherein the first contact pads and second contact pads are electrically connected to the semiconductor substrate between the gate lines by penetrating the first insulating layer;

forming a second insulating layer to cover the first contact pads and the second contact pads;

forming bit lines, wherein the bit lines cross over the gate lines and are electrically connected to the second contact pads by penetrating the second insulating layer;

forming a third insulating layer to cover the bit lines;

selectively etching the third insulating layer to form a band-type opening, wherein the band-type opening crosses the bit lines and exposes the first contact pads;

forming a conductive layer on the third insulating layer to fill the band-type opening;

patterning the conductive layer to form individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer in a direction of the bit line and a body that is electrically connected to a first contact pad; and

forming a storage electrode on each of the storage electrode contact bodies.

2. (Original) The method as claimed in claim 1, wherein the first contact pads are arranged in a direction of the gate line in a first column defined by a first and second gate line, and the second contact pads are arranged in a direction of gate line in a second column defined by the second and a third gate line.

3. (Original) The method as claimed in claim 1, wherein the band-type opening extends in a direction of the gate line.

4. (Original) The method as claimed in claim 1, wherein the band-type opening is formed to expose the first contact pads and surrounding first insulation layer that are disposed between the gate lines.

5. (Original) The method as claimed in claim 1, wherein a width of the band-type opening is greater than a width of the first contact pad.

6. (Original) The method as claimed in claim 5, wherein the band-type opening is formed to a width which allows a portion of the second insulating layer to remain on portions of the two gate lines adjacent to the second contact pads.

7. (Original) The method as claimed in claim 1, wherein forming the band-type opening comprises:

forming a band-type first photoresist pattern on the third insulating layer to expose portions of the third insulating layer which cover the first contact pads; and

selectively etching the exposed portions of the second insulating layer by using the band-type first photoresist pattern as an etch mask.

8. (Original) The method as claimed in claim 1, wherein forming the bit lines further comprises:

forming a capping insulating layer to cover the bit lines; and

forming spacers on sidewalls of the bit lines, wherein the capping insulating layer and the spacers prevent damage to the bit lines during the etching process.

9. (Original) The method as claimed in claim 8, wherein patterning the conductive layer is carried out by using the top surface of the capping insulating layer as an etch stopper.

10. (Original) The method as claimed in claim 1, wherein the conductive layer is a conductive polysilicon layer.

11. (Original) The method as claimed in claim 1, wherein patterning the conductive layer further comprises:

forming a second photoresist pattern on the conductive layer to partially expose portions of the conductive layer overlapping the bit lines and portions of the conductive layer overlapping the second contact pads disposed between the gate lines; and

etching the exposed portions of the conductive layer by using the second photoresist pattern as an etch mask.

12. (Original) The method as claimed in claim 1, wherein extensions of two adjacent storage electrode contact bodies, between which the bit line is disposed, extend in opposite direction from each other.

13. (Original) The method as claimed in claim 1, wherein the storage electrode contact body is formed such that a width of the extension in a direction of the bit line is greater than that of the body.

14. (Original) The method as claimed in claim 1, wherein the storage electrode contact body is formed such that the width of the extension in a direction of the bit line is greater than the extension in a direction of the gate line.

15. (Original) The method as claimed in claim 1, wherein the storage electrodes are formed such that most adjacent storage electrodes, between which the bit line is disposed, are arranged at an angle from the bit line.

16. (Original) The method as claimed in claim 1, wherein the two adjacent storage electrodes are arranged at an angle from the bit line or the gate line.

17. (Original) The method as claimed in claim 1, wherein the storage electrode is formed in a 3-dimensional cylindrical shape.

18. (Original) The method as claimed in claim 1, wherein the storage electrode is formed to occupy a circular, elliptical, or rectangular area.

19. (Original) The method as claimed in claim 1, wherein forming the storage electrode further comprises:

forming an electrode supporting layer to cover the storage electrode contact bodies;

forming a mold layer on the electrode supporting layer;

patterning the mold layer to form a mold, wherein the mold forms the storage electrode into a 3-dimensional shape;

forming a conductive layer on the mold;

patterning the conductive layer to separate the conductive layer into individual storage electrodes; and

selectively removing the mold.

20. (Original) The method as claimed in claim 19, wherein the electrode supporting layer further includes an etch stop layer that is used as an etch stopper when the mold is removed.

21. (Original) A method for manufacturing a semiconductor device comprising:

selectively etching an insulating layer formed on a semiconductor device to form a band-type opening, wherein the band-type opening crosses bit lines and exposes first contact pads which are electrically connected to an active region in the semiconductor device;

forming a conductive layer on the insulating layer to fill the band-type opening;

patterning the conductive layer to form individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the insulating layer in a direction of the bit line and a body that is electrically connected to a first contact pad; and

forming a storage electrode on each of the storage electrode contact bodies.

22. (Original) The method as claimed in claim 21, further comprising forming second contact pads which are electrically connected to the active region and the bit lines, wherein the first contact pads are disposed in a first column defined by a first and a second gate line, and wherein the second contact pads are disposed in a second column defined by the second and a third gate line.

23. (Original) The method as claimed in claim 21, wherein the band-type opening extends in a direction of the gate line.

24. (Original) The method as claimed in claim 21, wherein the band-type opening is formed to expose the first contact pads disposed between the gate lines.

25. (Original) The method as claimed in claim 24, wherein a width of the band-type opening is greater than a width of the first contact pad.

26. (Original) The method as claimed in claim 25, wherein the band-type opening is formed to a width which allows a second insulating layer to remain on portions of the gate lines adjacent to the second contact pad.

27. (Original) The method as claimed in claim 21, wherein extensions of the storage electrode contact bodies separated the bit line extend in opposite direction from each other.

28. (Original) The method as claimed in claim 21, wherein the storage electrode contact bodies are formed such that a width of the extensions in a direction of the bit line is greater than that of the body.

29. (Original) The method as claimed in claim 21, wherein the storage electrode contact body is formed such that the width of the extension in a direction of the bit line is greater than the extension in a direction of the gate line.

30. (Original) The method as claimed in claim 21, wherein the storage electrode is formed in a 3-dimensional cylindrical shape.

31. (Original) The method as claimed in claim 21, wherein the storage electrode is formed to occupy a circular, elliptical, or rectangular area.

32. (Original) The method as claimed in claim 21, wherein forming the storage electrode comprises:

forming an electrode supporting layer to cover the storage electrode contact bodies;

forming a mold layer on the electrode supporting layer;

patterning the mold layer to form a mold, wherein the mold forms the storage electrode into a 3-dimensional shape;

forming a conductive layer on the mold;

patterning the conductive layer to separate the conductive layer into individual storage electrodes; and

selectively removing the mold.

33. (Original) The method as claimed in claim 32, wherein the electrode supporting layer further includes an etch stop layer that is used as an etch stopper when the mold is removed.